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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,661	08/29/2003	Takao Moriwaki	402767	7786
23548	7590	04/15/2005	EXAMINER	
LEYDIG VOIT & MAYER, LTD			NGUYEN, KHANH V	
700 THIRTEENTH ST. NW				
SUITE 300			ART UNIT	PAPER NUMBER
WASHINGTON, DC 20005-3960			2817	

DATE MAILED: 04/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/650,661	MORIWAKI ET AL. 
	Examiner	Art Unit
	Khanh V. Nguyen	2817

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 04 February 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1,2 and 4 is/are rejected.
- 7) Claim(s) 3 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

**DETAILED ACTION**

***Response to Arguments***

Applicant's arguments with respect to claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Bailey et al. (5,654,672).

Regarding claims 1, 2, Bailey et al. (Fig. 3) disclose an active bias circuit for Class-AB amplifier comprising: a transistor (23A) can be read as semiconductor amplification element having a voltage supply (VCL) which can be read a first power source; and an isolation stage (22) can be read as a bias circuit for biasing the semiconductor amplification element (23A), wherein the bias circuit is supplied with a second voltage (VCC) which can be read as a second power source, the second power source (VCC) is connected to the first power source (VCL) via a transistor (31) which

can be read as a semiconductor element, and the idle current of the semiconductor amplification element (23A) changes in response to a change in the voltage supplied by the first power source (VCL).

Regarding claim 4, wherein the semiconductor amplification element (23A) is a transistor, a transistor (31) can be read as a bias circuit, and a reference voltage stage (21) can be read as a temperature compensation circuit having the function thereof.

Claims 1, 2, 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Moriwaki et al. (6,750,718).

Regarding claims 1, 2, Moriwaki et al. (Figs. 1-4) disclose a power amplifier comprising: a transistor (1) can be read as semiconductor amplification element having a voltage supply (7) which can be read a first power source; and a bias circuit (3) for biasing the semiconductor amplification element (1), wherein the bias circuit is supplied with a second voltage (6) which can be read as a second power source, the second power source (6) is connected to the first power source (7) via a transistor (10) which can be read as a semiconductor element, and the idle current (Ic) of the semiconductor amplification element (1) changes in response to a change in the voltage supplied by the first power source (7).

Regarding claim 4, wherein the semiconductor amplification element (1) is a transistor, a transistor (10) can be read as a bias circuit, and resistor (9) together with diode-connected transistors (23, 24) can be read as a temperature compensation circuit having the function thereof.

Claims 1, 2, 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyazawa (6,566,954).

Regarding claims 1, 2, Miyazawa (Fig. 2) discloses a high frequency amplifier bias circuit comprising: a transistor (21) can be read as semiconductor amplification element having a voltage supply via (212) which can be read a first power source; and a bias circuit (2) for biasing the semiconductor amplification element (21), wherein the bias circuit is supplied with a second voltage (25) which can be read as a second power source, the second power source (25) is connected to the first power source (212) via a transistor (22) and resistor (20) which can be read as a semiconductor element, and the idle current of the semiconductor amplification element (21) changes in response to a change in the voltage supplied by the first power source (212).

Regarding claim 4, wherein the semiconductor amplification element (21) is a transistor, a transistor (22) can be read as a bias circuit, and resistor (27) together with transistor (23) can be read as a temperature compensation circuit having the function thereof.

Claims 1, 2, 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Shih (6,492,874).

Regarding claims 1, 2, Shih (Fig. 4) discloses an active bias circuit comprising: a transistor (PA) can be read as semiconductor amplification element having a voltage supply (Vdd) which can be read a first power source; and a bias circuit (30) for biasing

the semiconductor amplification element (PA), wherein the bias circuit is supplied with a second voltage (Vabc) which can be read as a second power source, the second power source (Vabc) is connected to the first power source (Vdd) via a transistor (Q4) and resistor (RB) which can be read as a semiconductor element, and the idle current of the semiconductor amplification element (PA) changes in response to a change in the voltage supplied by the first power source (Vdd).

Regarding claim 4, wherein the semiconductor amplification element (PA) is a transistor, a transistor (Q4) can be read as a bias circuit, and resistors (R1, R2) together with transistors (Q1, Q2) can be read as a temperature compensation circuit having the function thereof.

#### ***Allowable Subject Matter***

Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 3 calls for, among others, the semiconductor element is a diode.

#### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh V. Nguyen whose telephone number is (571) 272-1767. The examiner can normally be reached from 8:00 AM - 3:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

Art Unit: 2817

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**KHANH VAN NGUYEN  
PRIMARY EXAMINER  
Art Unit: 2817**